An Agile stored ΣΔ sequence Fractional-N synthesiser

Rob Walkington and Dr. Paul Brennan

Department of Electronic and Electrical Engineering, University College London, Torrington Place, London, WC1E 7JE, United Kingdom

***Abstract* – The performance of ΣΔ Fractional-N frequency synthesisers has a direct relation to reference frequency. The upper limit on this reference frequency is often caused by the modulator, due to the limited speed achievable in fixed point hardware. Fixed point modulator feedback coefficients with limited precision also reduce modulator cycle length leading to unavoidable periodicity in the modulator output stream. To avoid these problems, a synthesiser has been designed which is particularly suited to burst mode systems such as DCS1800. The prototype described here stores pre-generated ΣΔ sequences in fast memory for each required channel, allowing a 'virtual' ΣΔ modulator operating at 240MHz to be implemented with a low cost FPGA and Flash memory.**

I. INTRODUCTION

Frequency hopping is commonly used to combat multipath fading in mobile radio. Requirements for agility and dynamic range are often severe and beyond the performance of an integer phase locked loop (PLL). DCS1800 is one such application, which commonly switches between two phase locked loops to achieve the required speed and spectral purity. This is a costly approach, which does not lend itself to integration due to the difficulty of isolating the loops.

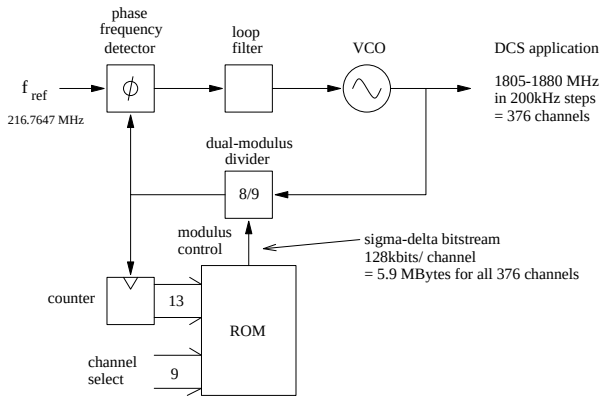

Fig 1. A Stored sequence fractional-N synthesiser

A recent approach which has proved popular in the quest for higher performance is a fractional-N synthesiser controlled by a sigma delta modulator [1]. This technique has the distinct advantage of high pass filtering and randomising the divider switching noise, so it can be easily removed by the loop filter.

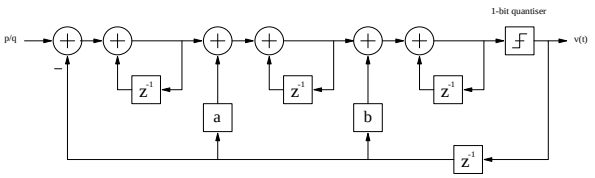

Fig 2. The 3rd order sigma delta modulator

A significant restriction on the performance of current implementations of such a synthesiser is often the modulator speed. Bottlenecks in operation speed are caused by hardware adders and multipliers and become worse as the data width increases, leading to a trade off between speed and precision. The use of fixed point feedback coefficients has a particularly damaging effect on modulator performance as it results in a reduction in the randomising of the modulator output, leading to shorter limit cycles and more in band tones. It would also be advantageous to be able to adjust modulator coefficients to suit the synthesised frequency, as the coefficients could then be optimised for each section of the band.

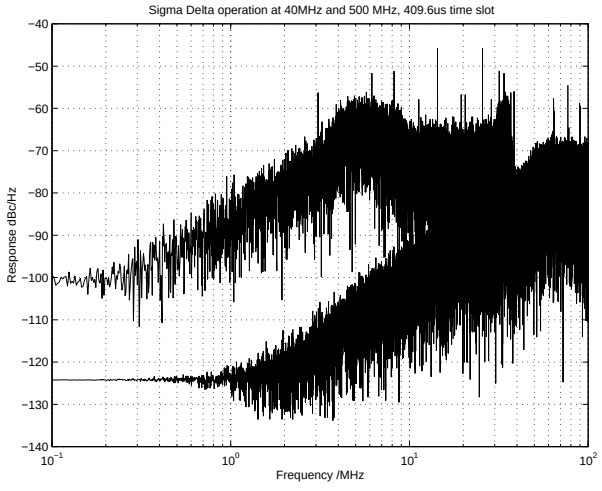

Fig 3. The effect of reference frequency on modulator NBPM referred to the loop output.

By exploiting the nature of frequency hopping systems, fabrication of a hardware sigma delta modulator can be avoided completely and instead an optimised sigma delta sequence for each required

channel stored in fast memory [2]. Making the stored sequence as long as the time slot length ensures no undesirable truncation effects. This also allows reference frequencies of several hundred MHz which provides a significant increase in the noise spreading performance of the modulator. This paper describes simulation and implementation of such a synthesiser.

II. Sigma Delta Fractional-N synthesisers

Fig 1. Shows an outline of a stored sequence synthesiser. A dual modulus divider placed in the feedback path is switched in a continuous manner to give an average division ratio between N and N+1. Fractional division allows a larger reference frequency for a given loop output resolution resulting in reference spurs further from the carrier which are less demanding to filter out, the ultimate aim being to widen the loop bandwidth and achieve much faster channel changing.

Figure 2 shows a block diagram of a third order sigma delta modulator. The modulator output is a pulse width modulated representation of its instantaneous input. Using a DC input to the modulator and one bit quantisation the feedback loop ensures that the average value at the modulator output equals that at the input, but a high pass response will be applied to the switching noise. By modelling the quantiser as a separate additive source the suppression of quantisation noise can be written using masons rule:

$$\frac{Y(z)}{N(z)} = \frac{(z-1)^3}{z^3-(2+a+b)z^2+(3+a+2b)z \quad -1-b} \qquad (1)$$

Where N(z) is the noise added due to the quantiser, Y(z) is the resulting noise at the output and a and b are negative feedback coefficients. Setting a and b equal to minus 1 gives a high pass characteristic of 60dB/ decade although in a real modulator instability results, leading to a requirement for more negative feedback and less noise suppression. Stability analysis is generally complicated due to the quantiser presence [3] although simulation can be used to obtain the best noise suppression consistent with stable operation.

Figure 3 shows the simulated dual modulus divider phase noise referred to the loop output for 40MHz and 500MHz sampling frequencies. Reduced power in ΣΔ output components at the higher sampling rate can be attributed to smaller bin width and increased ΣΔ noise suppression. The main improvement will be in the suppression of ΣΔ spurs, as the quantiser noise in Fractional-N applications is not white but harmonically related to the reference and synthesised frequencies by a process of intermod and aliasing. Storing the divider control sequence for each required channel in memory avoids hardware adders or multipliers making it feasible to fabricate sigma delta fractional-N loops with reference frequencies up to the GHz range.

II. Simulation of stored sequence synthesiser

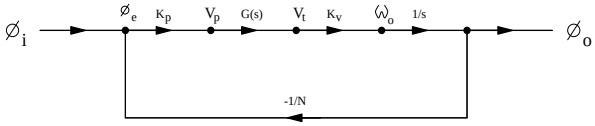

Fig 4. A generic synthesiser system

Figure. 4 shows a signal flow graph for a generic synthesiser system, where ϕ_o is the phase at the VCO output and ϕ_i is the phase at the reference input. K_p is the phase detector gain in Vrad^{-1}, G(s) is the loop filter transfer function and K_v is the VCO gain in rad/s/V. The additional 1/s term is due to the integrating action of the VCO and translates the output frequency ω_o to phase. With a third order type two loop filter, the closed loop response to phase variations at the divider input is given by [4]:

$$\frac{\phi_o(s)}{\phi_d(s)} = \left(\frac{\omega_n^2\psi s+\omega_n^3}{s^3+\omega_n\psi s^2+\omega_n^2\psi s+\omega_n^3}\right) = P(s) \qquad (2)$$
$$\left(\psi = \tan\phi_{PM} + \sec\phi_{PM}\right)$$

Where ϕ_{PM} is the loop phase margin. The N divider value is not required to calculate the loop phase noise response as the divider phase (ϕ_d) is referred to the divider output. Each time the divider is switched a step change in phase of plus or minus 2π is introduced at the divider output when V_{mod} changes between its two values. This will be added or subtracted from the cumulative sum of phase due to the divider switching. The phase at the start of the sigma delta sequence is set to zero to simulate an already locked loop. Therefore the loop phase response over the time slot can calculated. (3) removes the DC component of the modulator voltage, takes the cumulative sum of the voltage steps and converts them to phase steps, where n_s is the number of samples required at the chosen reference to cover the required time slot. V_{mod} is either 1 or 0:

$$\Delta\phi[n] = 2\pi\sum_{1}^{n_s}\left(V_{mod}[n] - \overline{V_{mod}}\right) \qquad (3)$$

Taking the spectrum of the phase modulation, a $2/n_s$ factor equalises the peak amplitudes on both sides of the FFT. A further zero-meaning of the phase steps is required to represent the case of a locked loop:

$$\phi_d(s) = \frac{2}{n_s}\,\mathrm{FFT}\left[\Delta\phi[n] - \overline{\Delta\phi[n]}\right] \qquad (4)$$

Phase noise spectral density at the synthesiser output

in dBc/Hz is found by applying the closed loop response, P(s), to the dual modulus divider phase modulation spectrum, $\phi_d(s)$, and applying dBc/Hz and NBPM scaling:

$$\phi_o(s) = \frac{2}{n_s}\phi_d(s)P(s)\frac{1}{2}\frac{F_{ref}}{n_s} \quad (5)$$

The results of such a spectral simulation are shown in figure 5, modelled for a fractionality of 0.65 and a third order sigma delta with feedback coefficients a and b of -9.345 and -8.459 respectively, obtained by optimisation of the maximum spur level in the output spectrum. On the same plot for comparison are ETSI DCS1800 masks for RMS phase noise in dBc/Hz (lower mask) and spurious in dBc. MASH modulator structures, whilst found to give much reduced noise very close to the carrier were found to not fit the masks as easily at critical points further out as the third order. It can be seen that close to the carrier the specification is more relaxed, any noise at this point being buried under that of the VCO and phase detector.

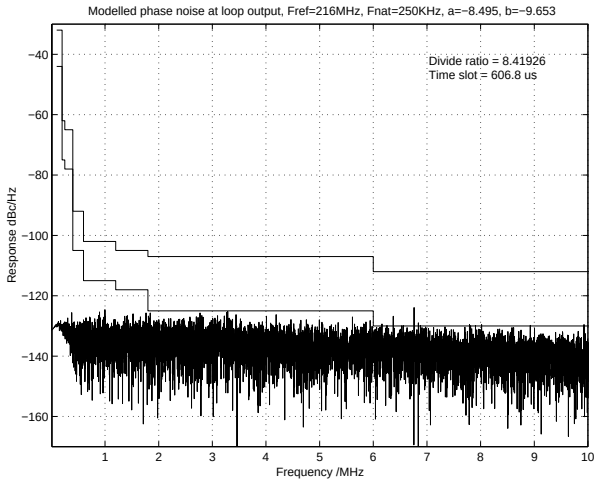

Fig 5. Simulated synthesiser phase noise spectral density, Fref = 200 MHz, 250Khz Natural frequency.

Fig 6. Shows a modelled 15 MHz hop with a third order type 2 loop with 250kHz natural frequency. Acquisition is to within 1kHz and $2x10^{-3}$ radians, referred to the VCO, within 10µs.

III. PROTOTYPE RESULTS

A discrete prototype has been fabricated on copper clad board using an ECL dual modulus divider and PFD, and a CMOS FPGA (10K30) with an 8Mbit flash EPROM. Output frequency range was 1248 to 1404MHz and a 250KHz loop natural frequency was used.

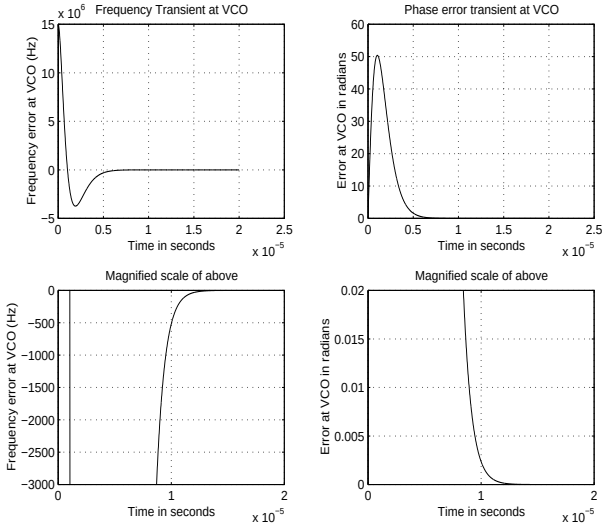

Fig 6. Simulated loop dynamics for a 15 MHz frequency hop.

The FPGA was capable of producing 250MHz data streams but reference frequency in this case was constrained to 156MHz by the 1.45GHz upper frequency limit of the ECL divider (MC12026A). Implementation in a fineline BiCMOS process would enable output frequencies over 3GHz.

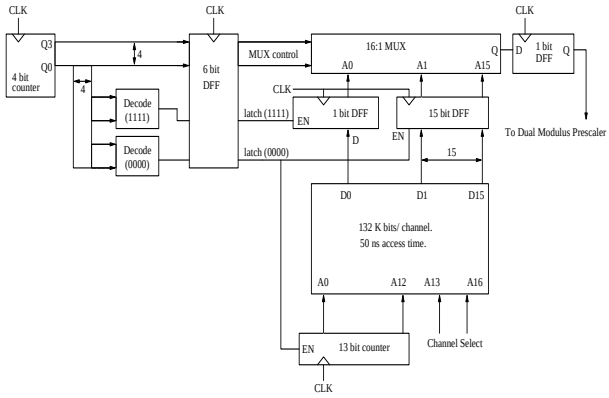

Fig 7. logic arrangement between memory and DMD.

Fig. 7 shows the logic arrangement for serialising the memory data and Fig 8. Shows a representative output spectrum for a fractional division ratio of 8.58. SFDR was better than 55dBc/Hz across the band. Higher than predicted spur levels were attributed to non-linearities in the loop components and were particularly dependent on the drive levels of the various stages. The difficulty of inter-stage coupling via the power supplies could be considerably improved with the use of more differential circuitry, particularly connections between saturating CMOS and non-saturating ECL sections. Fig. 10. Shows a measurement of RMS phase noise captured from the phase noise measurement facility of an HP8560E spectrum analyser. The lump in the response at 1MHz

was found to be due to a low speed op amp used in the active loop filter. Modulator noise cannot be seen due to the noise from the VCO, op amp and phase detector.

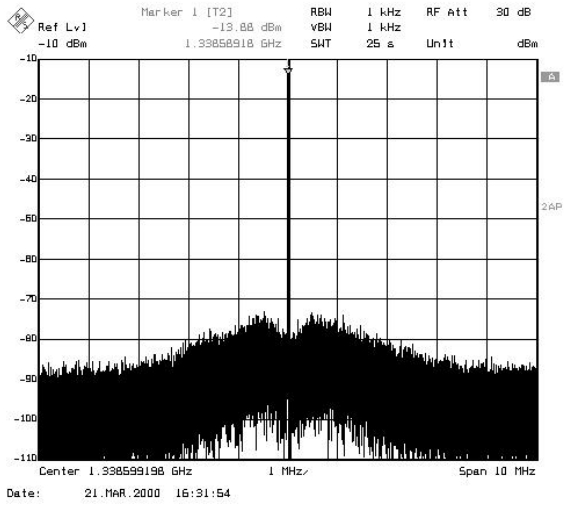

Fig 8. Prototype output spectrum with N=8.58.

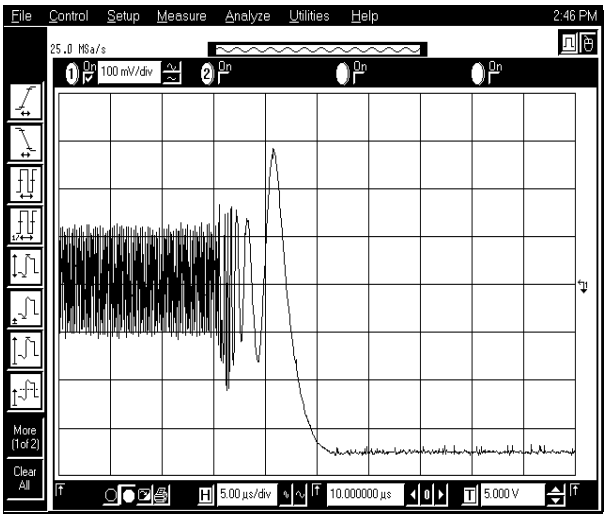

Fig 9. Measurement of 15MHz frequency hop to within 10° by mixing with synchronised signal generator.

Fig. 9 shows a 15MHz frequency hop in 10µs, measured by mixing the loop output with a synchronised signal generator of identical frequency and phase. The mixer output is fed to the oscilloscope, which is triggered from the channel change signal.

IV. Conclusion

It has been shown that by implementing the control of a fractional-N sigma delta synthesiser in memory it is possible to achieve significantly higher reference frequency operation for a given technology. This has

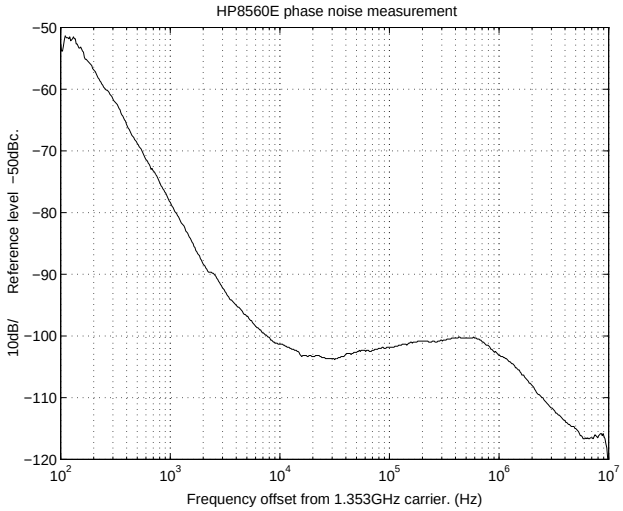

Fig 10. HP8560E RMS phase noise measurement of prototype.

the added advantages of allowing selective optimisation of modulator feedback across a band and reduced periodicity due to double precision simulation resolution. Implementing such a synthesiser in a fineline BiCMOS process would allow significant cost reductions in many applications and would allow reference frequencies of several hundred MHz, allowing very high performance noise spreading. In addition the technique shows good performance in continuous mode applications.

Acknowledgement

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References

[1] T.A.D. Riley, M. A. Copeland and T. Kwasnjeski, "Sigma-Delta modulation in fractional-N synthesis", *IEEE J. Solid-State Circuits*, vol 28 pp 553-559 May 1993.

[2] P.V.Brennan, R.Walkington, A.Borjak, & I. Thompson, "Very high-speed sigma-delta fractional-N synthesiser" IEE Electronics Letters, vol 36, issue 4, pp 298-300 February 2000.

[3] R. T. Baird, T. S. Fez, "Stability Analysis of High -Order Delta-Sigma Modulation for ADC's. *IEEE transactions on Circuits and Systems-2*, vol 41 pp 59-62, January 1994.

[4] P. V. Brennan, *Phase-locked loops, principles and practice*, Macmillan, 1996.